LM40A21
Dot Matrix LCD Unit

FEATURES

- STHC (Super Twisted High Contrast) Gray Type
- Low Power Consumption
- Thin, Lightweight Design Permits Easy Installation in a Variety of Equipment
- General-Purpose CMOS:
  - The Unit can be Easily Interfaced to a Microcomputer with Common 4-Bit and 8-Bit Parallel Inputs and Outputs
- Built-in Character Generator ROM, RAM, and Display Data RAM:
  - Character Generator ROM – 160 Different 5 × 7 Dot Matrix Character Patterns
  - Character Generator RAM – Eight Different, User-Programmed 5 × 7 Dot Matrix Patterns (Write Capability by Program)
  - Display Data RAM – 80 × 8 Bits
- Extensive Instruction Set:
  - Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Character Blink, Cursor Shift, and Display Shift
- Internal, Automatic Reset Circuit at Power-On
- Operates From a Single 5 V Power Supply and Incorporates an LCD Panel Which Provides a Highly Stable Display Over a Wide Range of Temperatures

DESCRIPTION

The SHARP LM40A21 Dot Matrix LCD Unit consists of a combination of a 5 × 7 dot 40-character 2-line dot matrix LCD panel, LCD driver, and controller LSI mounted on a single printed circuit board. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the unit is capable of efficiently displaying the desired characters under microcomputer control.

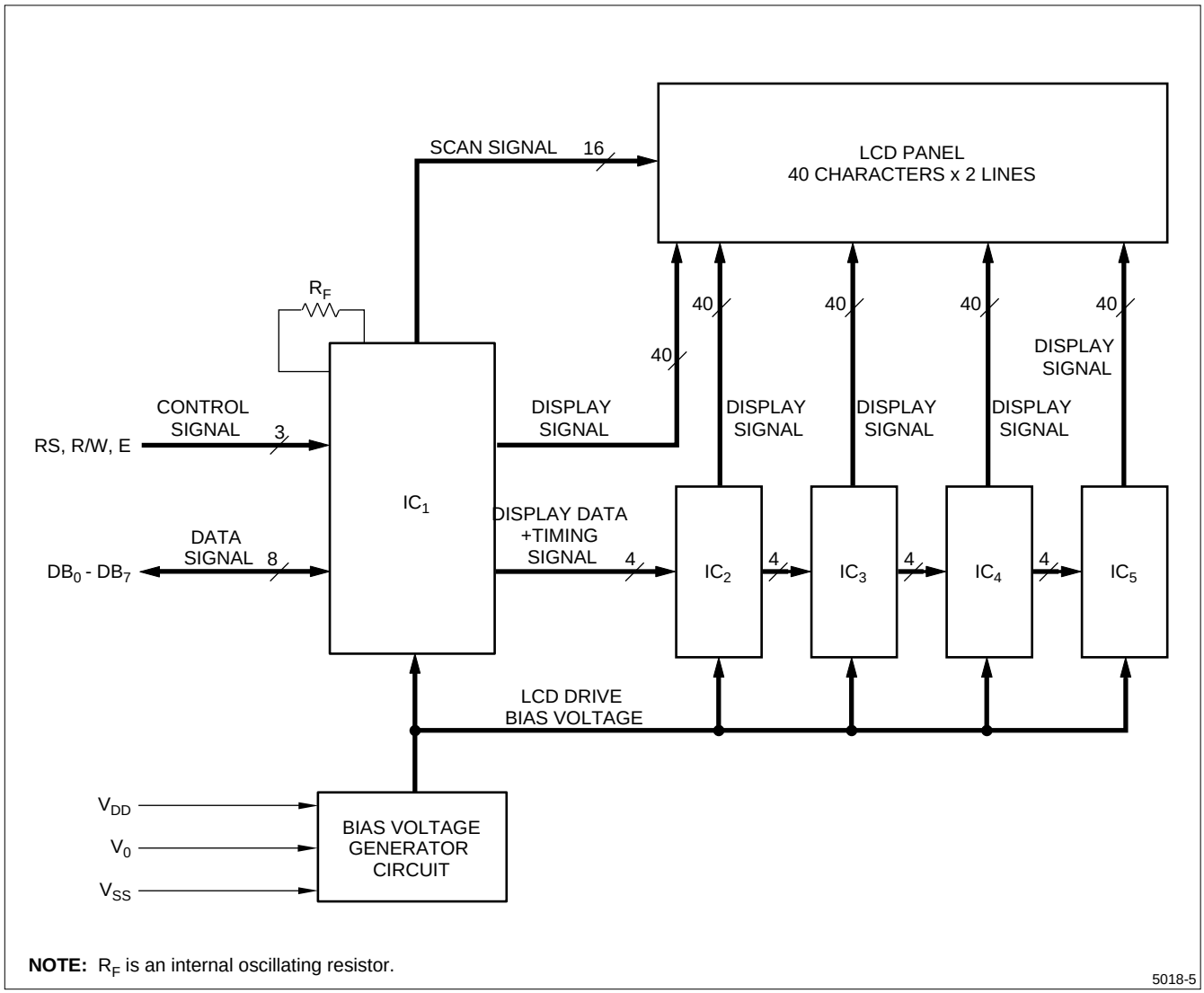


Figure 1. LM40A21 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTE
Outline Dimensions	182 (W) × 33.5 (H) × 11 max (D)	mm	–
Active Area	154.4 (W) × 15.8 (H)	mm	–
Display Format	40 characters × 2 lines	–	–
Character Format	5 × 7 dots, with cursor	–	–
Character Size	3.2 (W) × 4.85 (H) (5 × 7 dots)	mm	–
Dot Size	0.6 (W) × 0.65 (H)	mm	–
Dot Spacing	0.05	mm	–
Character Color	Dark blue	–	1
Backlight Color	Gray	–	1
Weight	Approximately 70	g	–

NOTES:
1. Due to the characteristics of the LC material, the colors vary with environmental temperature.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
$V_{DD} – V_{SS}$	Supply Voltage (Logic)	–0.3	6.5	V	–
$V_O – V_{SS}$	Supply Voltage (LCD Drive)	0	6.5	V	$VDD > V_0$
V_{IN}	Input Voltage	–0.3	V_{DD} +0.3	V	–
Tstg	Storage Temperature	–25	+70	°C	–
Topr	Operating Temperature	0	+50	°C	–

ELECTRICAL CHARACTERISTICS (t_A = 25°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE
$V_{DD} – V_{SS}$	Supply Voltage (Logic)		4.75	5.0	5.25	V	–
$V_O – V_{SS}$	Supply Voltage (LCD Drive)		–	0.5	–	V	V_{DD} = 5.0 V
V_{IL}	Input Voltage	'L'	–0.3	–	0.6	V	–
V_{IH}		'H'	2.2	–	V_{DD}	V	–
V_{OL}	Output Voltage	'L'	–	–	0.4	V	I_{OL} = 1.2 mA
V_{OH}		'H'	2.4	–	–	V	I_{OH} = –0.205 mA
I_{IL}	Input Leakage Current		–	–	1	µA	–
f_{OSC}	Internal Oscillating Frequency		–	160	–	kHz	–
I_{DD}	Supply Current		–	2.4	3.5	mA	V_{DD} = 5.0 V V_O = 0 V
P_D	Power Dissipation		–	12	17.5	mW	

INTERFACE TIMING (V_{DD} = 5.0 V ±5%, t_A = 0 to 50°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{CYCE}	Enable Cycle Time	1000	–	–	ns
PW_{EH}	Enable Pulse Width	450	–	–	ns
t_{ER}, t_{EF}	Enable Rise/Fall Time	–	–	25	ns
t_{AS}	RS, R/W Setup Time	140	–	–	ns
t_{AH}	Address Hold Time	10	–	–	ns
t_{DSW}	Data Setup Time	195	–	–	ns
t_{DDR}	Data Delay Time	–	–	320	ns
t_H	Data Hold Time (Write)	10	–	–	ns
t_{DHR}	Data Hold Time (Read)	20	–	–	ns

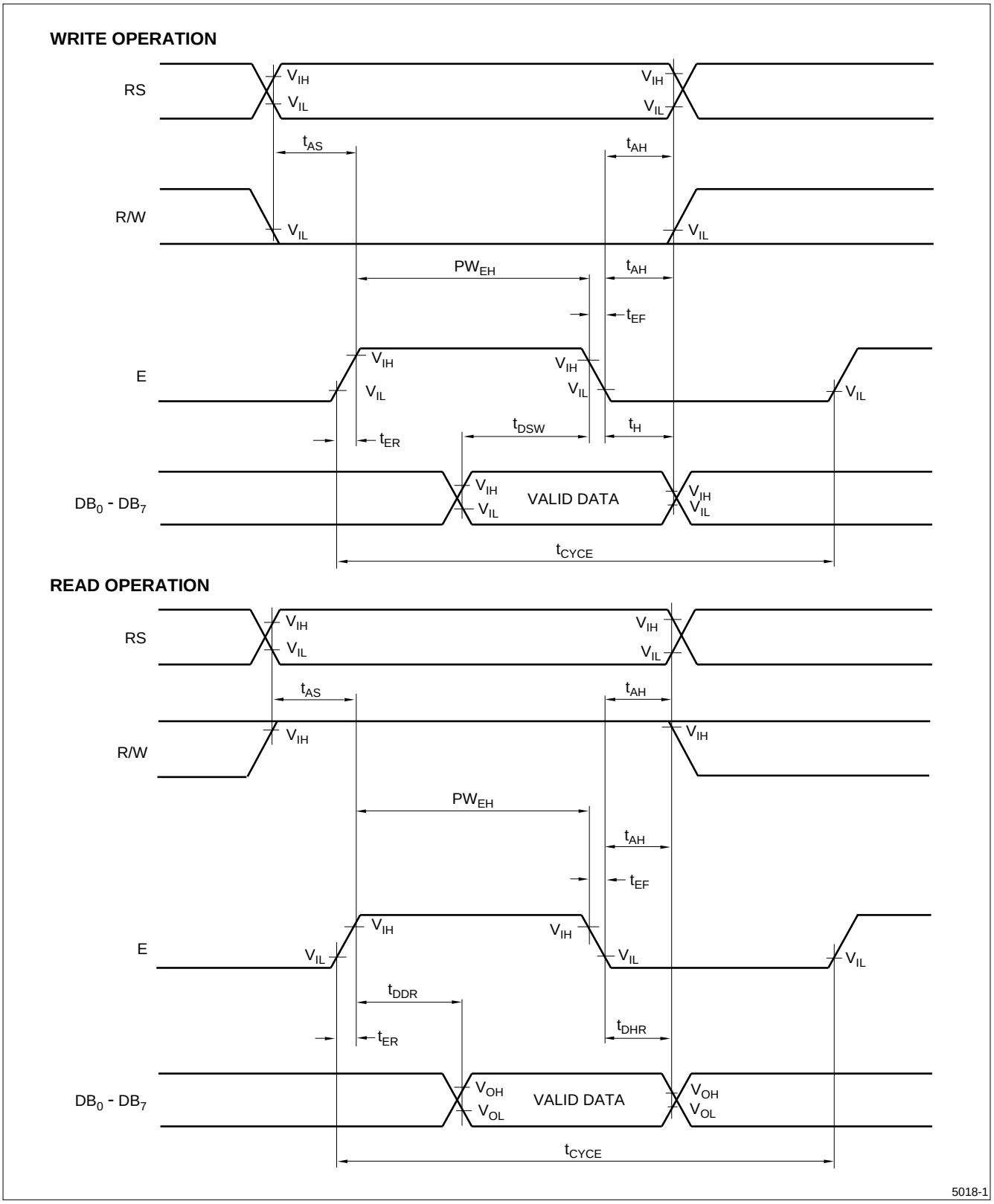


Figure 2. Interface Timing Chart

PIN CONNECTIONS

PIN NUMBER	SYMBOL	DESCRIPTION	CONNECTION
1	V_{SS}	Ground Potential	GND: 0 V
2	V_{DD}	Power Supply	+5 V Power Supply
3	V_O	Contrast Adjustment Voltage	Adjust the contrast by supplying voltage from 0 V to 5 V
4	RS	Register Select Pin	Control signal inputs
5	R/W	Read/Write Select Pin	
6	E	Enable Pin	
7	DB_0	Code I/O Data LSB	• Data bus signals • DB_7 may also be used to check the busy flag • DB_0 to DB_3 are not used when interfacing with a 4-bit micoprocessor
8	DB_1	Code I/O Data 2nd Bit	
9	DB_2	Code I/O Data 3rd Bit	
10	DB_3	Code I/O Data 4th Bit	
11	DB_4	Code I/O Data 5th Bit	
12	DB_5	Code I/O Data 6th Bit	
13	DB_6	Code I/O Data 7th Bit	
14	DB_7	Code I/O Data MSB	

OPTICAL CHARACTERISTICS (t_A = 25°C)

The following specifications are the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in θ = 0°.

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
$\theta_2 - \theta_1$	Viewing Angle Range	ϕ = 0°	$C_0 \geq 2.0$	60	–	–	degrees	1
θ_1		$\theta_1 < \theta_2$	C_0 = 2.0	–	–	-25		
θ_2				25	–	–		
$\theta_2 - \theta_1$		ϕ = 45° 315°	$C_0 \geq 2.0$	60	–	–		
θ_1		$\theta_1 < \theta_2$	C_0 = 2.0	–	–	-25		
θ_2				25	–	–		
C_0	Contrast Ratio	θ = 0°, ϕ = 0°		3.0	5.0	–	–	2
t_R	Response Speed – Rise	θ = 0°, ϕ = 0°		–	150	250	ms	3
t_D	Response Speed – Decay	θ = 0°, ϕ = 0°		–	150	250	ms	

NOTES:

1. The viewing angle range is defined as shown in Figure 3.
2. Contrast ratio is defined as follows:
   When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Figure 4.

   $$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non–select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

   Measurement wave length: λ = 580 nm.
3. When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test. method shown in Figure 4. The response characteristics of the photodetector output are measured as shown in Figure 5.

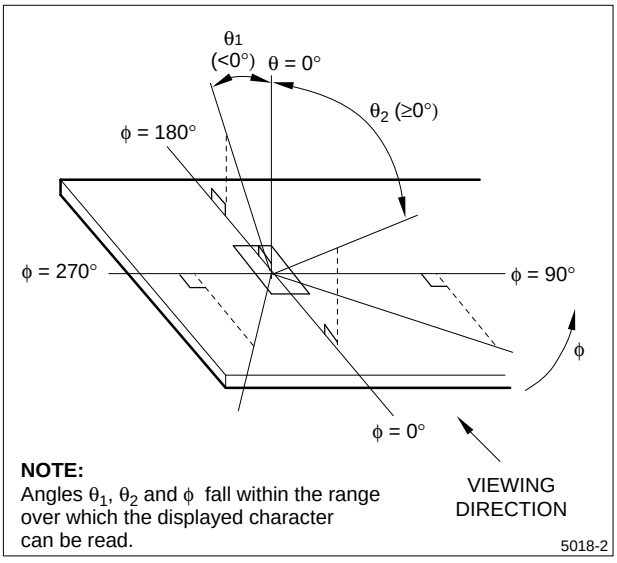


Figure 3. Definition of Viewing Angle

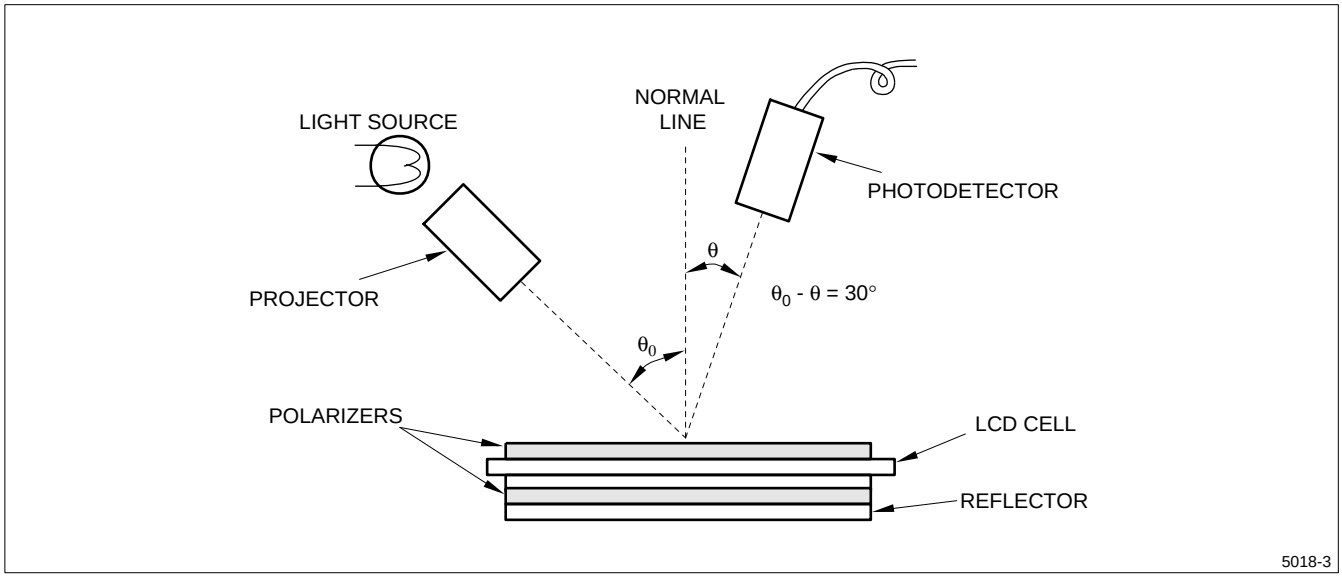


Figure 4. Optical Characteristics Test Method

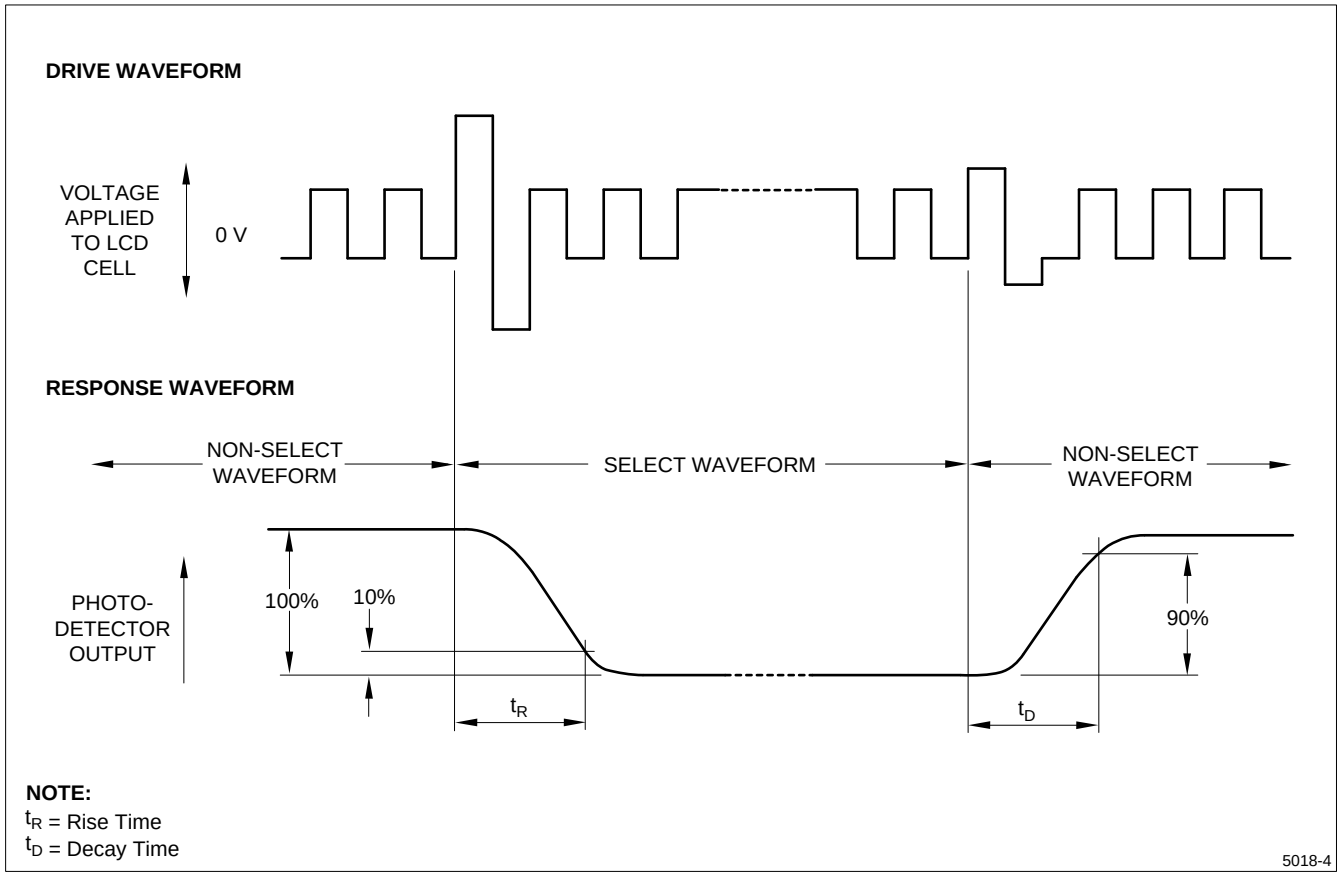


Figure 5. Definition of Response Time

PIN DESCRIPTION

V_{DD} and V_{SS} Pins

V_{DD} and V_{SS} pins are for the power supply. V_{SS} pin is grounded, and V_{DD} pin is supplied with +5 V. Each voltage necessary to drive LCD is generated in the unit.

RS Pin

The controller LSI contains two 8-bit registers: instructions register (IR) and data register (DR).

RS pin selects these registers. IR serves to store instruction codes for display clear, shift, etc. and address information for display data RAM (DD RAM), character generator RAM (CG RAM); DR serves to temporarily store data to be written into DD RAM and CG RAM.

'0': Instruction register (Write)
Busy flag register; address counter (Read)

'1': Data register (Read/Write)

R/W Pin

Read or write selection signal pin.

'0': Write

'1': Read

E Pin

Data read or write operation enable signal pin.

DB_0 to DB_7 Pins

Tri-state bidirectional data bus pins. The bus allows data to be transmitted to or received from the external circuit. DB_7 serves also as busy flag output. When the unit is interfaced to a microcomputer with 4-bit parallel outputs, DB_0 to DB_3 pins are not used.

V_0 Pin

Viewing angle is varied and contrast is adjusted by changing input voltage between +5 V to 0 V by applying bias voltage to the LCD driver.

INSTRUCTION SET

INSTRUCTION	CODES										DESCRIPTION
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Display Clear	0	0	0	0	0	0	0	0	0	1	Clears entire display area, restores display from shift, and loads address counter with DD RAM address 00H.
Display/Cursor Home	0	0	0	0	0	0	0	0	1	*	Restores display from shift and loads address counter with DD RAM address 00H.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specifies cursor advance direction and displays shift mode. This operation takes place after each data transfer.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specifies activation of display (D), cursor (C), and blinking of character at cursor position (B).
Cursor/ Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts display or moves cursor.
Function Set	0	0	0	0	1	DL	1	0	*	*	Sets interface data length (DL).
CG RAM Address Set	0	0	0	1	A_{CG}						Loads the address counter with CG RAM address. Subsequent data is CG RAM data.
DD RAM Address Set	0	0	1	A_{DD}							Loads the address counter with a DD RAM address. Subsequent data is DD RAM DATA.
Busy Flag/ Address Counter Read	0	1	BF	AC							Reads out busy flag (BF) and contents of address counter (AC).
CG RAM/ DD RAM Data Write	1	0	Write data								Writes data into DD RAM or CG RAM.
CG RAM/ DD RAM Data Read	1	1	Read data								Reads data from DD RAM or CG RAM.

NOTES:

I/D = 1: Increment
S = 1: Display shift
D = 1: Display ON
C = 1: Cursor ON
B = 1: Character at cursor position blinks
I/D = 0: Decrement
S = 0: Display freeze
D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Character at cursor position unblinks
S/C = 1: Display shift
R/L = 1: Right shift
DL = 1: 8 bits
BF = 1: During internal operation
S/C = 0: Internal cursor shift
R/L = 0: Left shift
DL = 0: 4 bits
BF = 0: End of internal operation

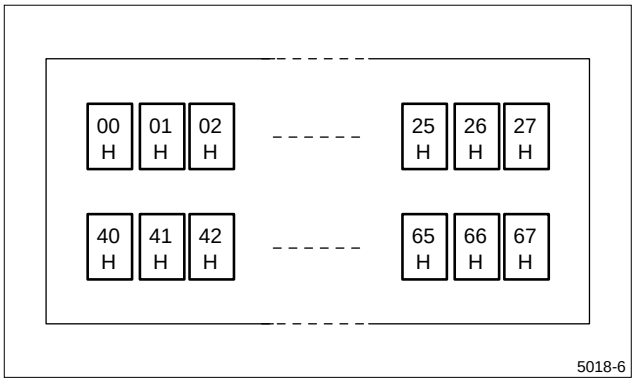


Figure 6. Display Address (When the Display is Not Shifted)

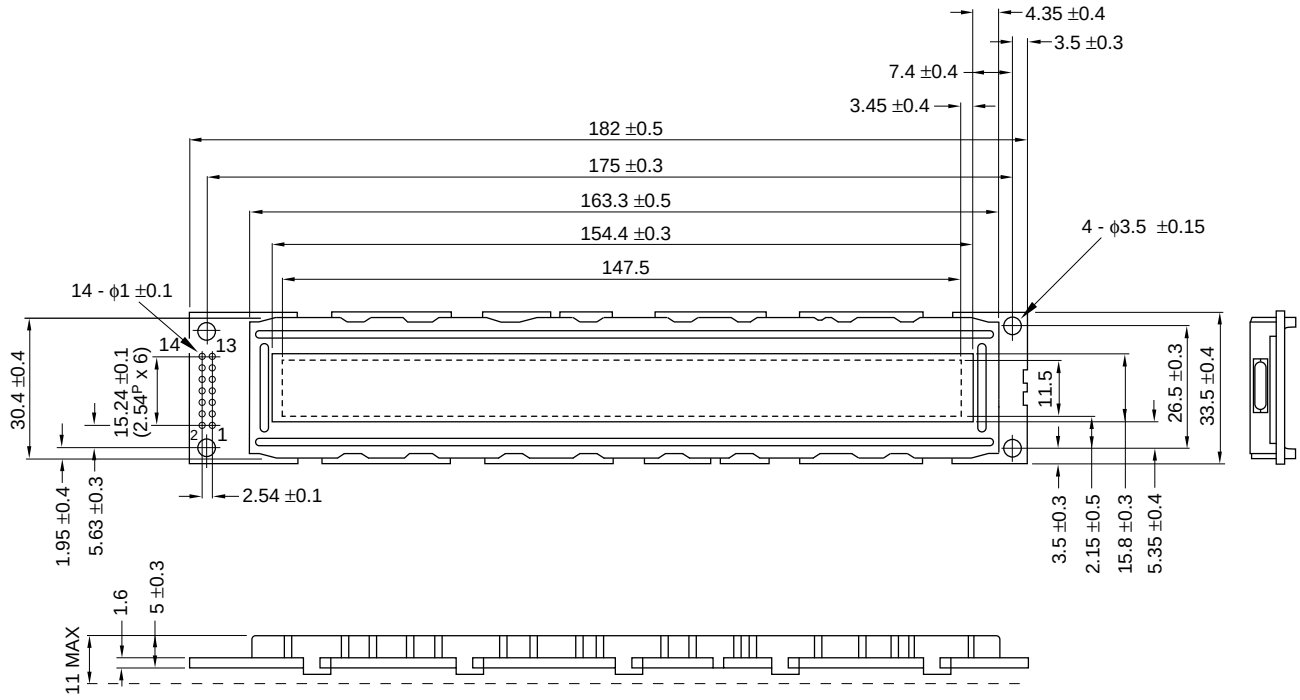
HIGH-ORDER / LOW-ORDER 4 BIT	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												*
xxxx0001	(2)												*
xxxx0010	(3)											*	
xxxx0011	(4)												
xxxx0100	(5)											*	
xxx0101	(6)												
xxx0110	(7)											*	
xxxx0111	(8)											*	
xxxx1000	(1)												
xxxx1001	(2)											*	
xxxx1010	(3)											*	
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												*

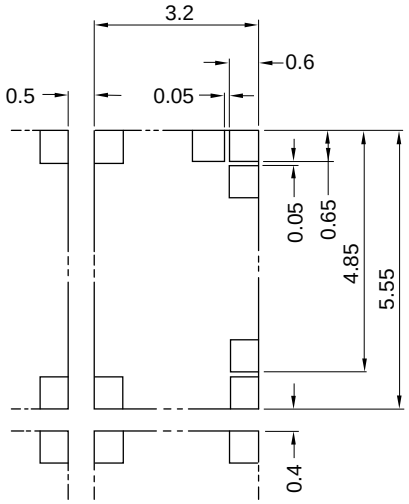
NOTES:

1. CG RAM is character generator RAM in which user-definable character patterns are stored.
2. X mark: prohibition of input.

Figure 7. Input Code vs. Character Pattern

OUTLINE DIMENSIONS





DOT SIZE
(S = 10/1)

PIN #	SIGNAL	PIN #	SIGNAL
1	V_{SS}	8	DB_1
2	V_{DD}	9	DB_2
3	V_O	10	DB_3
4	RS	11	DB_4
5	R/W	12	DB_5
6	E	13	DB_6
7	DB_0	14	DB_7

NOTE: Bezel plated with white-zinc.

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